IN THE CLAIMS

Please cancel claims 7 and 16, and amend claims 1, 2, 6, 8, 10, 11, 15, 19, 20, and 23 as indicated below.

1. (Currently Amended) A repeater device configured to repeat source synchronous data, said device comprising:

a first interface configured to receive the source synchronous data comprising a first data signal and a ~~corresponding~~ first clock signal;

a second interface configured to transmit source synchronous data; and

circuitry coupled to said first interface, wherein said circuitry is configured to:

utilize a reference clock signal and said first clock signal to generate a second clock signal;

utilize said second clock signal to latch said first data signal;

generate a third clock signal; and

utilize said third clock signal to transmit in a source synchronous manner a data signal and a clock signal corresponding to said ~~latched~~ first data signal and ~~a corresponding~~ the first clock signal via said second interface ~~in a source synchronous manner~~.

2. (Currently Amended) The device of claim 1, wherein said circuitry is configured to generate said third clock signal ~~in phase~~ out of phase with said first clock signal.

3. (Original) The device of claim 2, wherein said circuitry comprises a first circuit configured to:

receive said first clock signal;

receive said reference clock signal; and

generate said second clock signal to be approximately ninety degrees out of phase with said first clock signal.

4. (Original) The device of claim 3, wherein the first circuit is selected from the group consisting of: a delay locked loop, and a phase locked loop.

5. (Original) The device of claim 3, wherein said first circuit is further configured to:

generate a fourth clock signal approximately ninety degrees out of phase with said first clock signal; and

shift the phase of said generated second clock signal a first number of degrees to be approximately ninety degrees out of phase with said first data signal.

6. (Currently Amended) The device of claim 5, further comprising a second circuit configured to:

receive said reference clock signal;

receive said fourth clock signal; and

generate ~~a fifth~~ said third clock signal to be approximately in phase with said fourth clock signal.

7. (Cancelled).

8. (Currently Amended) The device of claim ~~7~~ 1, wherein said second circuit is selected from the group consisting of: a delay locked loop, and a phase locked loop.

9. (Original) The device of claim 5, wherein the first circuit is trainable to determine said first number of degrees.

10. (Currently Amended) A method for repeating source synchronous data, said method comprising:

~~receiving a first source synchronous data signal;~~

~~receiving a first clock signal corresponding to said first data signal;~~

receiving said source synchronous data comprising a first data signal and a first clock signal;

utilizing a reference clock signal and said first clock signal to generate a second clock signal;

utilizing said second clock signal to latch ~~said data corresponding to~~ said first data signal;

generating a third clock signal; and

utilizing said third clock signal to transmit in a source synchronous manner a data signal and a clock signal corresponding to said ~~latched~~ first data signal and ~~a corresponding~~ the first clock signal ~~in a source synchronous manner~~.

11. (Currently Amended) The method of claim 10, wherein said third clock signal is generated ~~in phase~~ out of phase with said first clock signal;

12. (Original) The method of claim 11, further comprising generating said second clock signal to be approximately ninety degrees out of phase with said first clock signal.

13. (Original) The method of claim 12, wherein said second clock signal is generated by a first circuit selected from the group consisting of: a delay locked loop, and a phase locked loop.

14. (Original) The method of claim 12, further comprising:

generating a fourth clock signal approximately ninety degrees out of phase with said first clock signal; and

shifting the phase of said generated second clock signal a first number of degrees to be approximately ninety degrees out of phase with said first data signal.

15. (Currently Amended) The method of claim 14, further comprising:
receiving said reference clock signal in a second circuit;
receiving said fourth clock signal in the second circuit; and
generating ~~a fifth~~ said third clock signal to be approximately in phase with said fourth clock signal.

16. (Cancelled).

17. (Original) The method of claim 15, wherein said second circuit is selected from the group consisting of: a delay locked loop, and a phase locked loop.

18. (Original) The method of claim 14, further comprising training a first circuit which generates said second clock signal to determine said first number of degrees.

19. (Currently Amended) A source synchronous system comprising:
a source device configured to convey source synchronous data comprising a first data signal and a ~~corresponding~~ first clock signal;
a repeater device coupled to said source device, wherein said repeater device comprises:
a first interface configured to receive said source synchronous data;
a second interface configured to transmit source synchronous data; and
circuitry coupled to said first interface, wherein said circuitry is configured to:
utilize a reference clock signal and said first clock signal to generate a second clock signal;
utilize said second clock signal to latch said first data signal;
generate a third clock signal; and

utilize said third clock signal to transmit in a source synchronous manner a data signal and a clock signal corresponding to said ~~latched~~ first data signal and ~~a corresponding~~ the first clock signal via said second interface ~~in a source synchronous manner~~; and

a destination device coupled to said repeater device, wherein said destination device is configured to receive said transmitted source synchronous data from said repeater device.

20. (Currently Amended) The system of claim 19, wherein said circuitry is configured to generate said third clock signal ~~in phase~~ out of phase with said first clock signal.

21. (Original) The system of claim 20, wherein said circuitry comprises a first circuit configured to:

receive said first clock signal;

receive said reference clock signal; and

generate said second clock signal to be approximately ninety degrees out of phase with said first clock signal.

22. (Original) The system of claim 21, wherein said first circuit is further configured to:

generate a fourth clock signal approximately ninety degrees out of phase with said first clock signal; and

shift the phase of said generated second clock signal a first number of degrees to be approximately ninety degrees out of phase with said first data signal.

23. (Currently Amended) The system of claim 22, wherein said circuitry further comprising a second circuit configured to:

receive said reference clock signal;

receive said fourth clock signal; and

generate ~~a fifth~~ said third clock signal to be approximately in phase with said fourth clock signal; and

wherein said circuitry is configured to utilize said ~~fifth~~ third clock signal to select for transmission in a source synchronous manner a data signal and a clock signal corresponding to said first data signal and the first clock signal.